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Paper Session I-C - Technology Advances and Developments in Low Power Gallium Arsenide for Space Applications

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Technological Advances and Developments in Low Power Gallium Arsenide for Space Applications

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Abstract

The evolution of gallium arsenide (GaAs) technology has developed to the point where it is quite suited for low power operation in space. The preliminary requirements for space-based integrated circuit applications are reviewed, and evidence that a GaAs technology known as complementary heterostructure field effect transistors (CHFETs) has proven to meet the demands of the space environment is presented. Further examples of how the complementary GaAs technology has demonstrated the potential for operation in the Gigahertz frequency range using power supply voltages at or below 2.5 Volts are presented. The analog and digital technological needs for space applications are identified and being met by complementary GaAs technologies when compared to commercial-off-the-shelf (COTS) electronics. Emphasis on the manufacturing costs of low power GaAs technologies when compared to those associated with COTS modified for space applications is addressed. Finally, information by both the Air Force and commercial sector concerning the need for low power GaAs technology insertion into future space-based systems is provided.

Introduction

This paper is intended to present low power GaAs technology options available for the design and fabrication of integrated circuits to be operated in space. Low power GaAs technology has taken an important role in meeting the rapidly growing sector of electronics for portable applications in the semiconductor industry. This is due to a superior power dissipation versus frequency relationship GaAs has when compared to Si-based electronics[1]. This is a critical factor when attempting to make performance improvements to low power electronics, such as an increased data rates or operating frequency, while making more efficient use of battery lifetime by striving for a decreased power supply level. Such attractive low power features must be met by GaAs if it is going to be suited for electronic operation in space.

One major thrust for low power GaAs for space has come from the inception of complementary GaAs devices, intended to mimic silicon (Si) CMOS, but have an increased operating frequency range due to the superior material properties possessed by GaAs. The concept of complementary GaAs technology was fostered through contractual and in-house research efforts at Wright Laboratory[2,3]. Complementary GaAs offshoots have been evolved towards space applications under government organizations such as Phillips Laboratory[3,4], National Security Agency[5], and Defense Systems Weapons Agency, and in the space commercial sector with companies such Boeing[6], Honeywell[1,2], Mayo Foundation[7], Motorola[8], National Semiconductor, and Systems & Planning Engineering Corporation (SPEC)[4].

The primary requirements for space-based integrated circuit applications are emphasized through radiation hardness (≥ 1Mrad), immunity to single event upset (SEU) phenomenon (≤ 10^{-8} Upsets/Bit-Day), and the capability of operating at a low supply voltage (V_{supply} ≤ 2.5 V). Evidence has been documented that GaAs devices and circuits have great potential for meeting the afore mentioned space environment requirements[9]. Additional developments in complementary GaAs technology have proven to meet the demands of the space environment, and have demonstrated the potential for operation in the Gigahertz frequency range using power supply voltages at or below 1.5 Volts[8,10,11,12]. Knowing that complementary GaAs is a technology suited to the space environment, additional packaging and shielding requirements can be minimized, providing additional weight savings to the spaceborne system. This can reduce further launch costs, making a very strong case for the use of complementary GaAs for space applications.

Space Environment Requirements

In the space-based operating environment, radiation exposure to electronics can lead to irreversible degradation effects[13]. The compromise of these electronics can occur from two different sources of radiation, (1) total dose ionizing radiation, and (2) transient radiation[14,15]. Total dose ionizing radiation is comprised of three components: proton dose, electron dose, and bremsstrahlung X-ray dose. Total dose radiation at low earth orbits is caused predominantly by protons within the Van Allen belt with energies greater than 30 keV. At geosynchronous altitude the proton dose is negligible and the bremsstrahlung dose dominates both the electron and proton doses.

With transient radiation, there is a production of free electrons and holes during a radiation pulse causing parasitic photocurrents or an upset event. Carrier generation is produced by high intensity gamma radiation or single energetic heavy ions. These photocurrents are induced at p-n junctions and Schottky barriers, and may be amplified through the device transistor action. The major effects to the electronic devices are classified as single particle events and are caused mainly by galactic cosmic rays in the space environment. Cosmic ray particles consist of 90% protons, but also include alpha particles and heavy ions. The kinetic energies of these particles range from 100 MeV to 100 GeV per nucleon. Three different events may occur in electronic devices: (i) single-event upset (SEU), (ii) single-event latchup (SEL), or (iii) single-event burnout (SEB). SEU produces a bit error, as for the case of an analog-to-digital converter without device degradation. SEL requires resetting the device power supply, while SEB produces irreversible device failure.

Additional requirements such as minimizing weight, volume, packaging, and power in spaceborne electronics have become increasingly important with the proliferation of small satellite programs within the defense and commercial space communities. Understanding that the components used in these systems must be both low power and radiation qualified, utilizing a semiconductor material like GaAs for space-based integrated electronics becomes reasonable. Fabrication of GaAs low power analog and digital circuits might increase the reliability of the electronics operating within the space environment.

GaAs Technology Development

Bearing in mind the aforementioned space environmental requirements, a strong case can be made for the use of GaAs-based devices and circuits in space applications. The total dose ionization hardness of GaAs FETs is very good compared to Si-based FETs since an oxide layer is not employed during fabrication [14]. Improved total dose response is evident by comparing the threshold voltage shifts for GaAs MESFETs which are in the millivolt range versus the one volt range for Si MOSFETs[9]. These threshold voltage shifts occur at total doses of 10^6 rad in Si MOSFETs, and at a higher dose of 10^8 rad in GaAs MESFETs.

With CHFET technology, there are additional performance enhancements from GaAs materials, but it is inherently radiation hard and maintains a low subthreshold gate leakage current, a very critical element of low power design and operation. Radiation testing has been documented for both digital and analog CHFET circuits, resulting in very little degradation in the circuit performance. SEU test results using heavy ion and proton analysis on a 1k CHFET SRAM demonstrated bit upset rates of 5.9 X 10^{-6} errors/bit-day - a two orders of magnitude improvement when compared with a similar GaAs MESFET circuit[10]. Operational amplifiers remained fully functional following a neutron irradiation total dose of 1.1 X 10^{15} cm^{-2}, and demonstrated only slight variations in open loop gain, leakage current and rise time[11,12].

More recently, improvements to complementary GaAs have been made at Motorola using their CGaAs™ process through the addition of a low temperature GaAs (LTG) buffer layer grown underneath the active device regions[8]. CGaAs™ devices with LTG were shown to have a significant improvement in the cross-section performance versus linear energy transfer (LET), and could be tuned for excellent SEU resistance (LET >20), possibly eliminating SEL[4]. This is depicted in Figure 1, where the determined SEU rate for the LTG wafers was 10^{-9} upsets/bit/day measured at the operating frequency of 800 MHz. In addition, the 0.5 μm p-channel CGaAs™ devices displayed significant improvements in their subthreshold characteristics, a problem which plagues all short channel complementary devices[16]. This also implies that deep submicron (< 0.5 μm) complementary GaAs technology is feasible lending itself to higher frequency, low power applications.

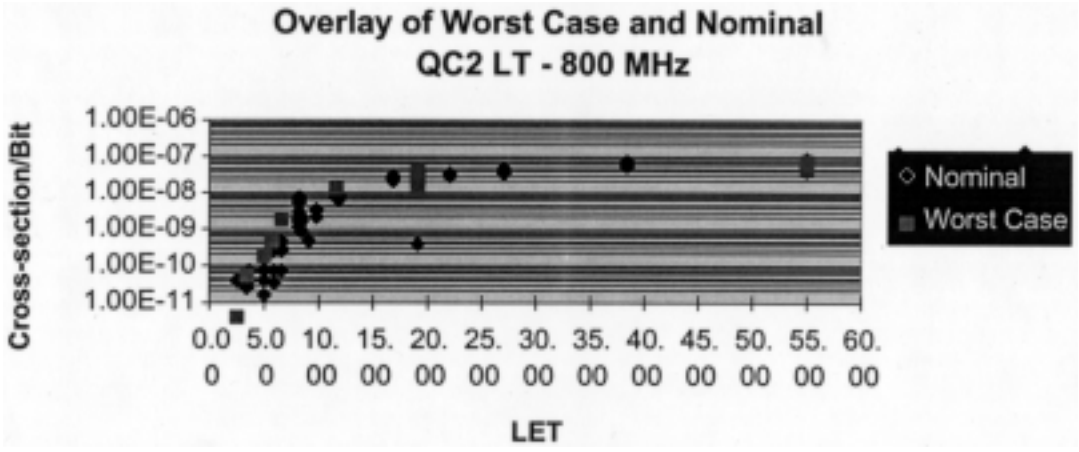

Figure 1

Fig. 1. SEU cross sections versus LET for CGaAs™ technology with LTG buffer tested at 800 MHz.

Recognizing that Si-CMOS devices and circuits have now demonstrated the capability to operate in the RF regime[17,18], it becomes imperative to examine low power GaAs technologies for RF designs[19]. Since complementary GaAs has met the space environment requirements of being both radiation hardened and operating with a low power supply, demonstration of a complementary GaAs RF device process was not a difficult task. This RF process could easily leverage many of the existing GaAs process fabrication techniques such as monolithic passive elements, allowing for efficient circuit designs.

A novel analog-based fabrication process known as *X*s-MET™ (pronounced kismet, which uses the Greek letter chi, *X,* and stands for complementary heterostructure integrated single metal transistor), was recently developed at Wright Laboratory for the purpose of extending the performance inherent to GaAs, while utilizing the low power and radiation immune characteristics of a complementary technology[3]. In addition to a GaAs device structure, the *X*s-MET™ manufacturing technique can be utilized to develop small scale complementary analog circuits. The *X*s-MET™ process is aimed at minimizing fabrication process variations which can impede performance and reliability, two important aspects of electronics operation in space.

The *X*s-MET™ process merges a substitutional-gate, ion-implanted process with a combined optical/electron-beam lithography process to yield a complementary device pair from a single metalization step with a T-shaped submicron gate length features. *X*s-MET™ 's unique process feature is derived from the effective use of a single layer of silicon nitride (Si_3N_4) to perform four process tasks which are: 1) a substitutional gate, 2) an implant sidewall, 3) an implant screen, and 4) a secondary mask, and is summarized pictorially in Figure 2. The *X*s-MET™ fabrication process only requires eleven process steps and seven mask levels to produce a submicron complementary pair and is easily extended to incorporate interconnect lines for the manufacturing of simple analog circuits.

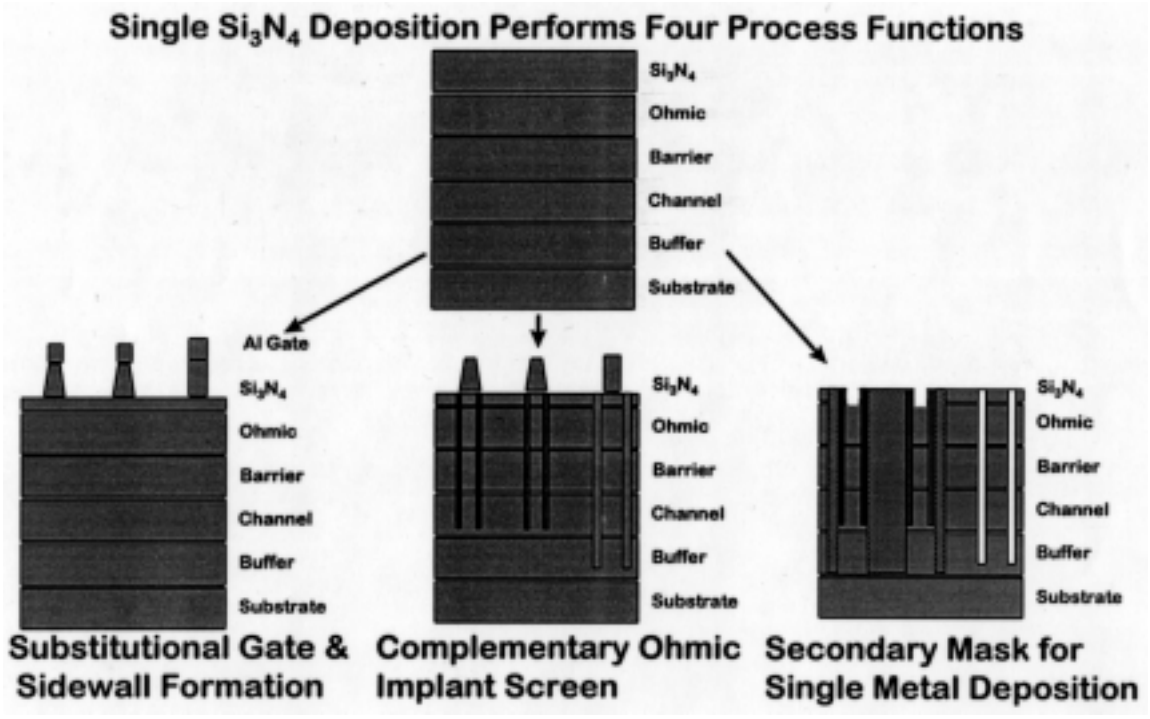

Figure 2

Fig. 2. *X*s-MET™ process description highlighting the four process functions accomplished through a single Si_3N_4 deposition.

Low Power GaAs Applications

I. Digital

Motorola has successfully applied the incorporation of the LTG buffer to some current products which have been space qualified. KG 207 is a Motorola dual-channel 900 Mbps serial data transmitter, composed of CGaAs™ LSI and SSI level digital logic components and employs a circuit hardening approach through differential pair partitioning to obtain an SEU level of 10^{-9} Upsets/Bit-Day when tested using a supply voltage range between 1.2 and 1.5 Volts as depicted in Figure 3[21]. The R222 project teamed the National Security Agency (NSA) and the Mayo Foundation with Motorola to develop and demonstrate a multichip module (MCM) comprised of 15 data generation/acquisition circuits tied to a single clock distribution circuit utilizing 0.7µm CGaAs™[7]. From this collaborative effort came the development of a 0.7µm CGaAs™ design library, a high performance packaging arrangement and advances in the level of integration to Motorola's CGaAs™ technology to demonstrate a 16 channel signal distribution circuit designed with 170K transistors[8].

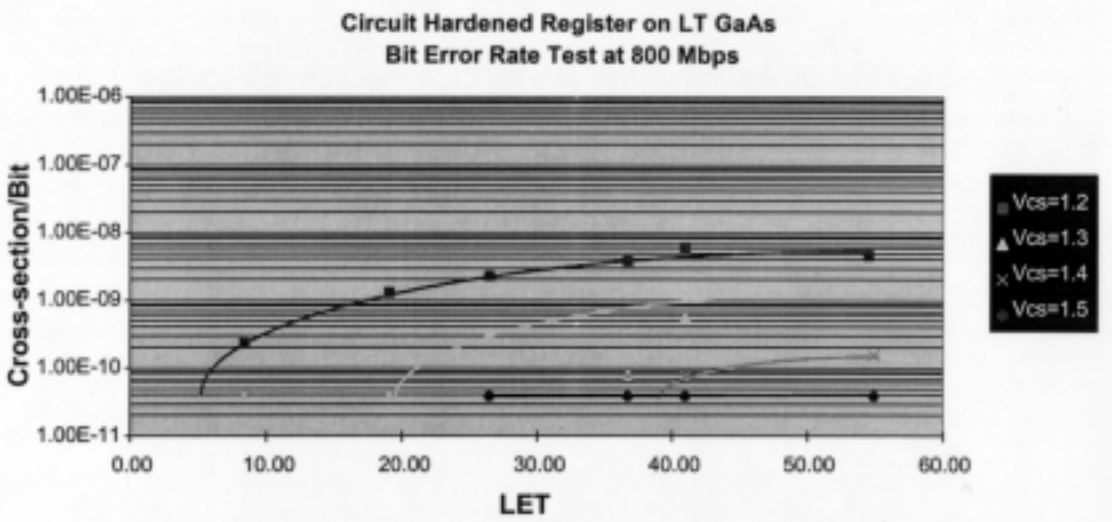

Figure 3

Fig. 3. SEU levels versus LET for Motorola's KG-207 chip under four different drain bias conditions.

II. Analog

Presently, Phillips Laboratory and Wright Laboratory are collaborating on an effort develop low power GaAs analog electronics for space. From a space requirements point-of-view, the radiation tolerance level of the operational amplifier does dictate the maximum performance of the system. This becomes the key reason for developing a circuit fabrication process which can be both flexible and durable in a harsh operating environment. The use of flexible analog signal processors (FASPs) is also a prudent choice for space applications due to their multi-tasking capabilities from a single design. The FASP is also a means by which the design-to-fabricate cycle time can be reduced. In simplifying the design of the analog circuit, greater reliability can be achieved during operation.

This effort couples the FASP design concept with the *X*s-MET™ process, and the result was the design of a single metal two-stage cascode operational amplifier. The threshold electrical

requirements for the *X*s-MET™ operational amplifier are to have a unity gain bandwidth of 1 GHz, a supply voltage of 2.5 Volts, and a 100 dB gain. The preliminary RF characterization of *X*s-MET™ devices, fabricated in a ground-signal-ground arrangement, with two gate fingers 0.4 mm in length by 50 mm wide, displayed a cutoff frequency (f_t) range of 2-5 GHz[3]. Process improvements are being implemented to increase the f_t value, and the first lot of packaged *X*s-MET™ devices are undergoing on-ground radiation testing. This proved to be a successful first demonstration of a single metal complementary GaAs for RF applications.

Future Directions

Motorola is continuing to advance its CGaAs™ process, by moving to deep submicron features (0.4 μm), and increasing the overall transistor density of its digital circuits[20]. The Celestri™ project is Motorola's proposed space-based broadband communications system linking low earth orbit (LEO) and geostationary earth orbit (GEO) satellites to new and existing terrestrial networks for a seamless communication service[21]. CGaAs™ integrated circuits will make up a large portion of the Celestri™ payload because of its space qualified track record. At the same time, emerging spaceborne multispectral and hyperspectral sensors and high data rate communications systems are driving requirements for ever faster on-board processors. This has forged a new project with Motorola, SPEC, and the Air Force Research Laboratory to design, fabricate, characterize and space-qualify a reconfigurable field programmable gate array (FPGA). Designed by SPEC in Motorola's 0.7 μm CGaAs™ technology, the FPGA has 402K transistors, and the simulation results showed a 350 MHz operating frequency using a power supply voltage of 1.5 Volts, and an estimated power dissipation of 800 mW[22]. The layout of the FPGA is shown in Figure 4, and has a die size of 50 mm^2. Once fabrication and testing is completed, a potential use for such a chip may be in the area of adaptive computing, where configurable memory is a must.

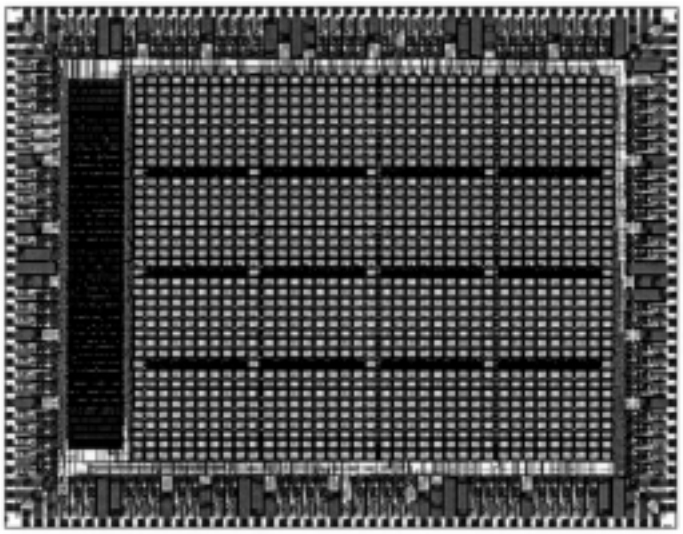

Figure 4

Fig. 4. SPEC's reconfigurable FPGA layout in Motorola's 0.7 μm CGaAs™.

The Air Force Research Laboratory has begun an initiative to develop a space-based radar antenna technology with drivers for low power operation, while maintaining high efficiency. This would push the technology areas of low power GaAs mixed signal designs and advanced DC/RF multi-level packaging. The Air Force could leverage much that has been developed for GaAs

MMICs, but modify the designs to meet the specific requirements of low power, space operation. Heterojunction bipolar transistors (HBTs) as well as field effect transistor (FET) device technologies will more than likely be implemented in MCM configurations in order to carry out some of the functions of the antenna array such microwave power and signal generation, and analog-to-digital signal conversion.

Conclusions

Both the military and commercial sectors have identified the requirements for low power space electronics, which can be met through the use of complementary GaAs. Continued evolution of low power GaAs technologies will be needed for advanced technology demonstrations of space-qualified analog and digital circuits as performance levels for space telecommunications improve. Funding for a portion of the work performed in this paper came from project number FMBD-96-514-WL, and contract number F29601-96-C-0016.

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