

# Design parameters of a power management system for an emerging Medical Artificial Intelligence of Things (MAIoT) technology

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## Abstract

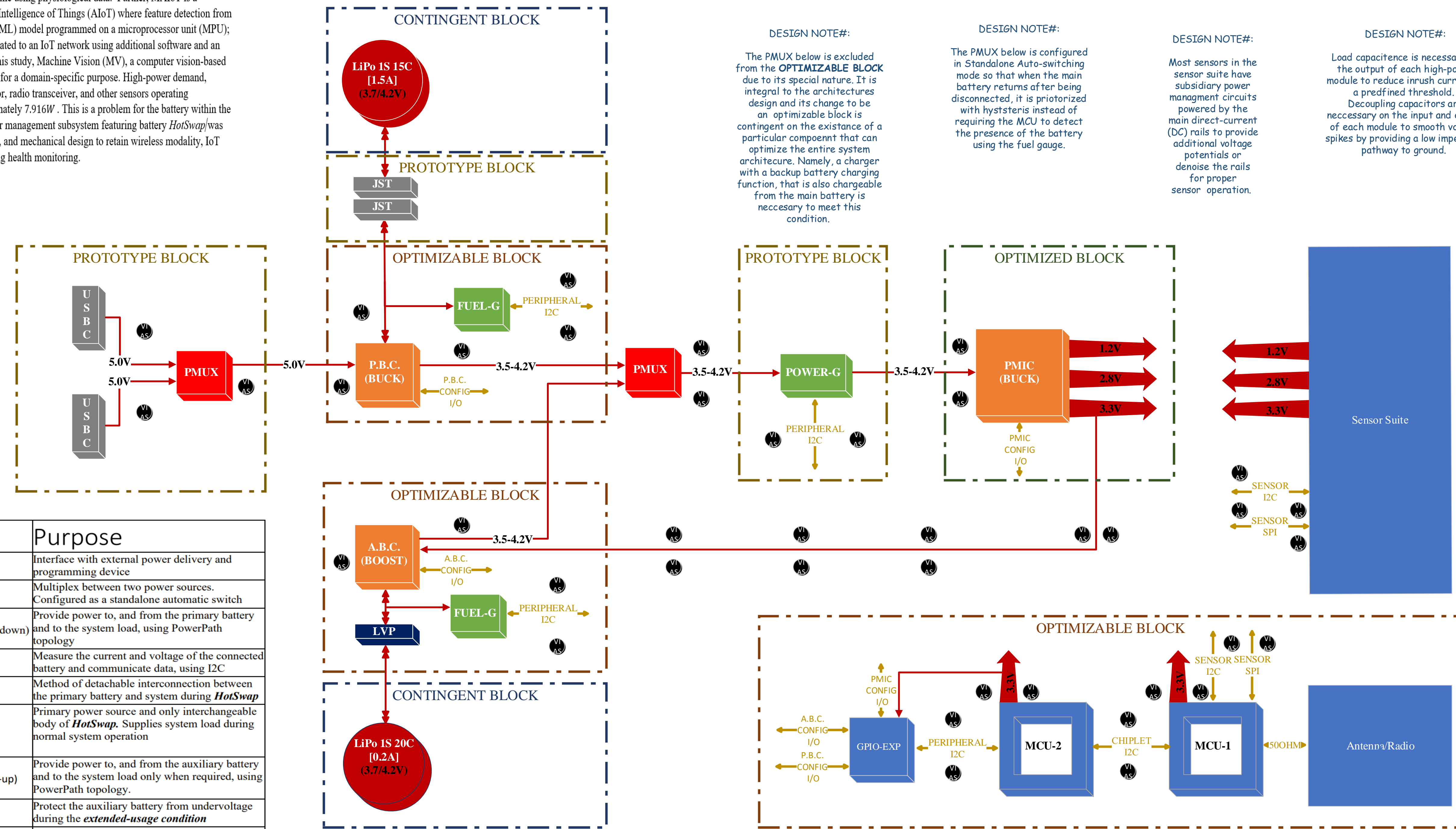
Though concurrent growth of technologies can sometimes lead to discord, often they lead to the meshing of ideas to form a new frontier of study, collaboration, and innovation. Recently, the inelastic collision of technologies has begotten a new frontier, called Medical Artificial Intelligence of Things (MAIoT), edge-inferencing, encompassing the knowledge from Internet of Things (IoT) and Artificial Intelligence (AI), just targeted toward medicine using physiological data. Further, MAIoT is a discipline-focused subcategory of Artificial Intelligence of Things (AIoT) where feature detection from sensor data is done by a Machine Learning (ML) model programmed on a microprocessor unit (MPU); sequentially, inference results are communicated to an IoT network using additional software and an integrated circuit (IC) radio transceiver. In this study, Machine Vision (MV), a computer vision-based form of ML, is used to enhance camera data for a domain-specific purpose. High-power demand, specifically, from the camera, microprocessor, radio transceiver, and other sensors operating simultaneously, generates a load of approximately 7.916W. This is a problem for the battery within the targeted handheld device. Therefore, a power management subsystem featuring battery *HotSwap* was conceived by combining hardware, software, and mechanical design to retain wireless modality, IoT connectivity, and practitioner dexterity during health monitoring.

### DESIGN NOTE#:

*HotSwap* Subsystem Architecture comprised of IC's for space optimization on a dense PCB. Architecture is dependent on the design requirements. The most imposing requirement being the need to charge the auxiliary cell from the primary cell.

Component	Purpose
USB-C	Interface with external power delivery and programming device
PMUX	Multiplex between two power sources. Configured as a standalone automatic switch
P.B.C.	Provide power to, and from the primary battery and to the system load, using PowerPath topology
FUEL-G	Measure the current and voltage of the connected battery and communicate data, using I2C
JST	Method of detachable interconnection between the primary battery and system during <i>HotSwap</i>
LiPo 1S 15C [1.5A]	Primary power source and only interchangeable body of <i>HotSwap</i> . Supplies system load during normal system operation
A.B.C.	Provide power to, and from the auxiliary battery and to the system load only when required, using PowerPath topology.
LVP	Protect the auxiliary battery from undervoltage during the <i>extended-usage condition</i>
LiPo 1S 20C [0.2A]	Auxiliary power source and integral fixed body of <i>HotSwap</i> . Supplies system load during the <i>extended-usage condition</i>
POWER-G	Measure the power requirement of the system load and communicate data, using I2C
PMIC	Distribute power to the system load by generating multiple DC voltage rails at variable potentials via a supervisory IC
GPIO-EXP	Provides additional I/O pins controllable through an I2C bus when host controller GPIO is limited
MCU-2	Manage peripheral (accessory) ICs. Contribute to the system load
MCU-1	Manage image processing, AI inference and streaming. Contribute to the system load
Antenna/Radio	Matching network and chip antenna w/ or w/o secondary IC. Contribute to the system load
Sensor Suite	Comprised of various sensors, e.g. camera. Contribute to the system load

Block Type	Definition
Prototype Block	Only present during early research and development TRL, or serves as a placeholder
Contingent Block	Dependent on a system requirement or technology availability or existence
Optimizable Block	Comprised of components that can be optimized in some way such as combining submodules into one all-encompassing module that exists
Optimized Block	Gone through intense iteration. Only susceptible to change when the integration of a new component into system engenders new knowledge or design requirements. Typically, this event is apparent with the development of the final circuit belonging to the deployable device, high TRL. Otherwise, the status of the block remains constant.



### DESIGN NOTE#:

The PMUX below is excluded from the **OPTIMIZABLE BLOCK** due to its special nature. It is integral to the architecture design and its change to be an optimizable block is contingent on the existence of a particular component that can optimize the entire system architecture. Namely, a charger with a backup battery charging function, that is also chargeable from the main battery is necessary to meet this condition.

### DESIGN NOTE#:

The PMUX below is configured in Standalone Auto-switching mode so that when the main battery returns after being disconnected, it is prioritized with hysteresis instead of requiring the MCU to detect the presence of the battery using the fuel gauge.

### DESIGN NOTE#:

Most sensors in the sensor suite have subsidiary power management circuits powered by the main direct-current (DC) rails to provide additional voltage potentials or denoise the rails for proper sensor operation.

### DESIGN NOTE#:

Load capacitance is necessary on the output of each high-power module to reduce inrush current to a predefined threshold. Decoupling capacitors are necessary on the input and output of each module to smooth voltage spikes by providing a low impedance pathway to ground.

### DESIGN NOTE#:

A micro rechargeable lipo is used instead of a supercapacitor due to its greater specific energy.

### DESIGN NOTE#:

The embedded LiPo battery is inaccessible to the user, and it is cycled and regulated so it needs a standalone LVP cutoff circuit in the event of the *extended-usage condition*, or user negligence.

### DESIGN NOTE#:

The bit address of the fuel gauges that use the I2C communication protocol can be changed via hardware, so identical microchips can remain on the same I2C bus. Another solution is to use an I2C expander.

### DESIGN NOTE#:

Vias provide a short path to ground which help to reduce crosstalk and stability of high current through a trace.

### DESIGN NOTE#:

Diagram only details VBUS DC power rails, and LOW/HIGH elementary logic connections for submodule configuration. Data lines are excluded from the diagram besides those relevant to the Primary Power Management System.