May 1st, 1:00 PM

Paper Session III-C - Technology Transfer of Military Space Microprocessor Development

C. Gordon
Space Mission Technology Division, Phillips Laboratory

D. King
Space Mission Technology Division, Phillips Laboratory

L. Byington
Space Technology Directorate, The Aerospace Corporation

D. Lanza
Maxwell Technologies Federal Division

Technology Transfer of Military Space Microprocessor Development

C. Gordon*, D. King*, L. Byington+, and D. Lanza#

*Space Mission Technology Division, Phillips Laboratory, Kirtland AFB NM 87117
+Space Technology Directorate, The Aerospace Corporation, Albuquerque, NM 87119
#Maxwell Technologies Federal Division, Albuquerque, NM 87106

Abstract

Over the past 11 years Phillips Laboratory has led the development of microprocessors and computers for USAF space and strategic missile applications. As a result of their programs, advanced computer technology is available for use by civil and commercial space customers as well. The Generic VHSIC Spaceborne Computer (GVSC) program began in 1985 at the USAF Phillips Laboratory to fulfill a deficiency in the availability of space-qualified data and control processors. GVSC developed a radiation hardened multi-chip version of the 16-bit, Mil-Std 1750A microprocessor. The follow-on program to the GVSC, the Advanced Spaceborne Computer Module (ASCM) program, was initiated by Phillips Laboratory to establish two industrial sources for complete, radiation-hardened 16-bit and 32-bit computers and microelectronic components. Development of the Control Processor Module (CPM), the first of two contract phases, completed in 1994 with the availability of two sources for space-qualified, 16-bit Mil-Std-1750A computers, cards, multi-chip modules, and integrated circuits. The second phase of the program, the Advanced Technology Insertion Module (ATIM), is currently scheduled to complete at the end of 1997. ATIM is developing two single board computers based on 32-bit reduced instruction set computer (RISC) processors. GVSC, CPM, and ATIM technologies are flying or baselined in the majority of today's DoD, NASA, and commercial satellite systems.

1. INTRODUCTION

Over the past 11 years, Phillips Laboratory has pioneered the development of space-qualified microprocessors and computers for USAF satellite and strategic missile applications. These products have been very successfully inserted into numerous Air Force and DoD space programs, and are baselined into major programs like MILSTAR, SBIRS, and GPS. This advanced computer technology has also been quickly transferred into civil and commercial space programs. Three major systems initiatives at Phillips Laboratory have contributed greatly to the availability of computer resources for both military and commercial satellite system designers: The Generic VHSIC Spaceborne Computer (GVSC) program, the Control Processor Module (CPM), and the Advanced Technology Insertion Module (ATIM). The CPM and ATIM efforts were actually completed as phases of a single program.

A number of objectives tied these major programs together and contributed to their wide insertion in commercial as well as military programs. A major objective of each program was producibility and qualifiability of the technology. This included integrated circuit yield enhancements and a thorough examination and demonstration of assembly and packaging processes. Also an objective was the demonstration of usable component-level products, such as support chipsets, I/O interfaces, and multichip packaging components. A third objective was to provide a complete package to the user, including tools needed to write actual control and payload applications The overall goal was to provide a “PC for space”, an obvious computer solution that makes custom computers for each satellite unnecessary. These objectives resulted in computer systems that, besides meeting military space system needs, are additionally marketable for civil and commercial satellites.

When the ATIM program ends in December of 1997, these objectives will be continued and extended in planned developmental efforts like the Phillips Laboratory’s Improved Space Computer Program (ISCP). (Note: For more information on the ISCP, there is another paper being presented at this conference titled, “Improved Space Computer Program: Advanced Processing for 21st Century Military and Commercial Satellites.”)

This paper provides an overview of each of these programs and reviews the broad scope of government, civil, and commercial programs that will be entrusting their success to these Phillips Laboratory products.

2. GENERIC VHSIC SPACEBORNE COMPUTER PROGRAM

In 1985, the Generic VHSIC Spaceborne Computer (GVSC) program began with two major objectives. The first objective was to establish at least two suppliers of producible, space-qualified, radiation-hardened, very high speed integrated circuits (VHSIC). The second objective was to prove the capability of the two suppliers by designing and fabricating 16-bit microprocessors implementing the MIL-STD-1750A avionics instruction set. By the end of the program in 1989, Honeywell Space Systems (Clearwater FL) and IBM Federal Systems (now Lockheed Martin Federal Systems, Manassas VA) had fabricated GVSC microprocessors conforming to the MIL-STD-1750A instruction set, and hardened to space and strategic radiation environments.

The GVSC was the first development of fully-hardened complex logic devices in VHSICˇI technology (1.0-1.2Êm design rules). By contrast with the later CPM and ATIM programs (discussed later), this was only a chip set development. It included hardware and software for breadboard demonstration, but no support chips, flight board hardware design, or software development environment. In parallel with the GVSC development, both contractors were additionally under a separate contract for the 64Kbit SRAM development.

Technical Achievements

The GVSC program was the first demonstration that a VHSIC-level bulk CMOS fab process could be hardened to military space levels, particularly in the areas of prompt dose and single-event upset. Both contractors met or exceeded the program goals of 106˘rad(Si) total dose, 109˘rad(Si) prompt dose, and 10-10˘errors/bit-day SEU. Interestingly, the evaluation leading to the downselect from five to two contractors showed that the two leading fab lines had SEU rates better than a competing fab line using CMOS/SOS technology.

Throughput of the chip sets (embedded in a demo breadboard) was measured at the SEAFAC verification facility at 3˘MIPS or better for both contractors. This was a substantial improvement over the 0.2-1.0 MIPS of previous space processors.

Technology Transfer

GVSC chip sets were delivered for use on MILSTAR and at least one other DoD program, but the chip sets have primarily been incorporated in CPM-derived board-level products. Use of those products has been substantial in both military and civilian space, as discussed below.

3. CONTROL PROCESSOR MODULE

Following completion of the GVSC microprocessor program in 1989, Phillips Laboratory began the Control Processor Module (CPM) program to build complete computer systems around the GVSC processors. The CPM was actually the first phase of the Advanced Spaceborne Computer Module (ASCM) contract, a new competitive procurement at Phillips Laboratory. The contract awards again went to Honeywell Space Systems and IBM Federal Systems (now Lockheed Martin Federal Systems).

CPM had two principal goals: implementing and refining the then-new Qualified Manufacturers List (QML) concept at the two fab lines, and producing fully supported space-qualifiable 16-bit computers. Building these complete computers involved developing complete processor, memory, I/O, and power converter capabilities. As with the GVSC program, emphasis was placed on producibility, both for the support and memory chips (1 micron CMOS interface chips and 256Kbit static RAM chips) and for the assembly and packaging processes.

The CPM program was a pathfinder for the QML concept, a qualification method that focuses on the manufacturers processes, and the way those processes are developed, rather than end-of-line part screening. QML is now the standard military electronics qualification method. QML uses statistical process control, and carefully designed and documented processes, to produce known-high-quality parts. In the context of semiconductor manufacturing, this means having key parameters of all process steps under statistical process control and continually working to keep the process centered and to reduce variability. As implemented under military specification MILƒMƒ38535, it also means having a controlled process for the design-to-physical layout transition to ensure that chip implements the intended design. The CPM program was the first application of QML to a rad-hard (and hence low-volume) fab line. It involved a considerable amount of independent verification testing, and considerable work by the contractors in implementing statistical process control and working on yield inhibitors.

Each contractor based its computer on its respective GVSC processor chip set, and added support chips for memory control, I/O, and system management. Remaining tasks included multi-chip modules for both memory and processor chips; board designs for processor, I/O, and memory; chassis design; software for a real-time operating system, initialization, and fault management; development of an Ada software development environment; and environmental testing including shock, vibration, temperature cycling, and EMI/EMC.

Technical Achievements

Both contractors successfully QML qualified their design and fab processes, and have upgraded that qualification to each new process level. Both box-level CPM designs successfully passed all qualification tests, including particularly severe vibration and EMI/EMC levels.

4. CPM TECHNOLOGY INSERTIONS

CPM technology has been baselined in many of today's Air Force and DoD satellite systems. Additionally, technology from these programs has been transferred to civil and commercial satellite developers. A general summary of these insertions is shown in figure 1. Several of these systems have already been successfully launched. These include:

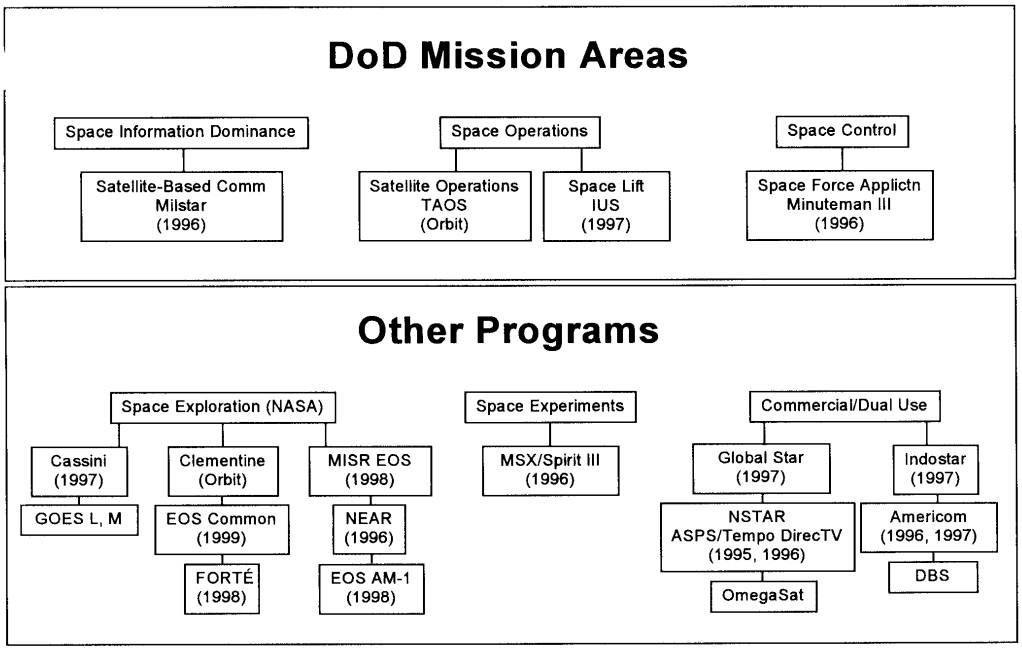

Figure 1. Programs that have flown or baselined CPM technology

∑ TAOS (Technology for Autonomous Satellites) Used the increased processing power made available by the CPM computer to demonstrate satellite autonomy.

∑ ClementineJoint SDIO/NASA satellite tested a variety of sensors in a lunar mapping mission. Use of standard components like CPM enabled deployment of the Clementine vehicle in less than two years.

5. ATIM TECHNOLOGY INSERTION MODULE

Now nearing completion are 32-bit single board computer systems under the Advanced Technology Insertion Module (ATIM) program (Phase II of the ASCM program). These systems incorporate the full complement of computer functions (processor, memory, and I/O) on a single 6" x 9" circuit card while maintaining interoperability with the CPM subassemblies. The ATIM computers extend the performance of previous space computers into the 32-bit arena by transferring and adapting existing comercial 32-bit reduced instruction set computer (RISC) processor technology. Processing power for these computers comes from the Honeywell Space Systems RH32 processor (developed at Rome Laboratory) and the IBM RISC/6000 (radiation hardened at Lockheed Martin Federal Systems). These processors are fabricated in radiation-

hardened submicron CMOS technologies, and are supported by interface chips exceeding 100,000 equivalent gates. The ATIM computers are built using the QML concepts pioneered under CPM.
Memory capabilities are also increased using 1 Mbit static RAM chips packaged in multichip modules for greatly increased density. I/O capabilities have been correspondingly increased. The ATIM computers will also come complete with advanced operating systems and sophisticated, user-friendly applications development environments. Software development has been greatly simplified by the adaptation of commercial operating systems and development environments that run on the commercial parent processors from which the ATIM processors were derived.

ATIM Technical Achievements
The ATIM program is demonstrating single board computers in the 20-40 MIPS throughput range. Backing up this processor performance is increased density in support chips and memories achieved through much higher levels of integrated circuit integration and advanced multichip packaging. Both of these advances are now available for technology transfer.

6. ATIM TECHNOLOGY INSERTIONS

As with the earlier GVSC and CPM programs, ATIM and its technologies are being used by civil and commercial customers for space qualified processing needs. The first launch of ATIM technology occurred in November 1996 with the Mars Pathfinder. Following that insertion are planned insertions in several NASA space and planetary exploration missions, including the New Millennium ventures, and at least four commercial systems. Additional ATIM insertions are outlined on the chart in figure 2.

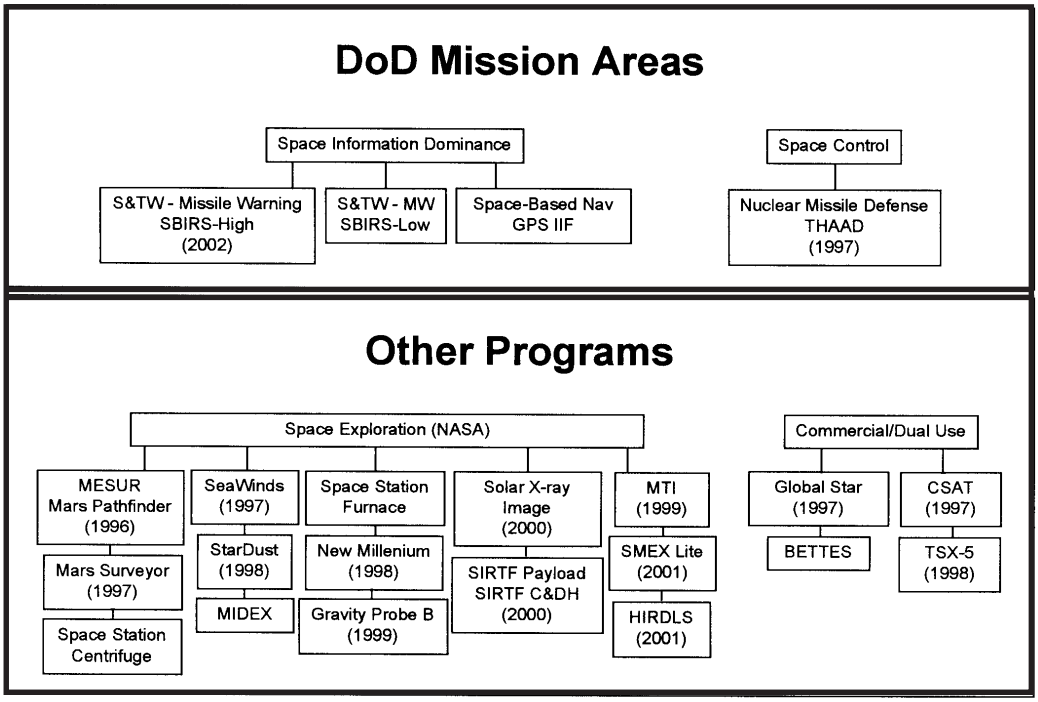

Figure 2. Programs that have flown or baselined ATIM technology

7. OTHER APPLICATIONS OF ASCM TECHNOLOGIES

While the previous discussions emphasized the wide application of variants of the ASCM computer designs, using primarily the same chips designed on ASCM, the ASCM semiconductor fabrication technology itself has been applied to the production of a wide variety of other devices for both military and civil space.

The rad-hard submicron SOI gate array technology developed by Honeywell on the ASCM program has an extremely high prompt-radiation-dose tolerance, a property needed for strategic missile applications. It also provides very high gate counts (300-400K gates) with much higher gate utilization than the previous bulk designs. The Air˘Force Ballistic Missile Office took advantage of these properties in an ongoing program to transition the older 5-chip GVSC processor set into a single-chip SOI design. This will give them the cost savings of replacing a multi-chip module with a single processor chip and the prompt-dose performance of SOI.

The good fab yields and convenient design tools of the SOI gate array led several non-Phillips˘Lab 32ƒbit processor programs to use it for their implementations. This includes the Rome˘Lab/TRW RHƒ32, the NASA Mongoose˘V, the Harris RH3000, and others.

Lockheed Martin Federal Systems has created a significant business in Actel-compatible field programmable gate arrays (FPGAs) and antifuse-based PROMs by adding antifuse design and fab (on another Phillips˘Lab program) to their basic ASCM rad-hard submicron capability. Two digital signal processor developments at Lockheed Martin are also based on that capability. Both contractors have used their space-qualified fab processes to build numerous special I/O and support chip designs for both military and civil space customers.

8. SUMMARY AND CONCLUSIONS

Through the success of the GVSC, CPM, and ATIM programs, Phillips Laboratory has established itself as the leader in the development of computers for space. GVSC, CPM, and ATIM technologies are flying or baselined in the majority of today's Air Force and DoD satellite systems. Additionally, technology from these programs has been transferred to civil and commercial satellite developers. Though not all NASA missions and few commercial missions have extreme radiation requirements like many military satellites, the availability of an off-the-shelf solution with a space heritage makes existing military technology attractive to civil and commercial developers.